REMARKS

Reconsideration and allowance of this application, as amended, are respectfully requested.

Claim Status

Claims 1-6 are in the application with claims 4-6 being withdrawn from consideration.

Prior Art Rejections

The prior art grounds of rejection are respectfully traversed.

Claims 1-3 stand rejected as being anticipated by Lin. Applicant respectfully disagrees. There are differences between our claimed inventions and Lin that are specifically called for in our claims. Thus, Applicant asks that the rejections be withdrawn.

Claim 1 calls for, in part:

> a ***device isolation film*** formed on a semiconductor substrate, the device isolation film having a groove that exposes a portion of the semiconductor substrate defining an active region and having ***substantially vertical profile*** with respect to the exposed portion of the semiconductor substrate;

Lin does not disclose a device isolation film having a vertical profile with respect to the semiconductor substrate, as required by our claim 1. Lin's isolation structure 424 neither has nor requires a vertical profile. Our device isolation film 32, on the other hand, requires a vertical profile because a side wall of the device isolation film 32 has a spacer 39 formed therein.

Claim 1 further requires:

> a ***gate electrode structure*** formed in a central portion of the active region of the semiconductor substrate and separated from the device isolation film, wherein the gate electrode structure further comprises:
>
> a stacked structure of a gate oxide film, a first gate electrode and a second electrode,

an oxide layer formed on a side wall of the first gate electrode, and

nitride spacers formed on the oxide layer on the sidewall of the **first gate electrode** and on a side wall of the device isolation film;

Lin does not teach a gate structure having a first gate electrode and a second gate electrode with a spacer 39 formed only on the first gate electrode 35. Spacers 437 of Lin are formed to bound the entire gate structure, including a polysilicon gate member 447, a metallization layer 443, and a silicon nitride layer member 484.

Lin's isolation structure 424 does not have a spacer formed thereon. However, our isolation film 32 has a spacer 39 formed thereon.

A third insulating film 45 in our inventions does not correspond to Lin's layer 470. The third insulating film 45 fills and planarizes the space between the gate electrode and the device isolation film. However, Lin's layer 470, although having a planarized surface, covers the isolation structure 424 rather than covering the space between gate structure 440 and the isolation structure 424.

Given the differences, clearly set forth in our claims, continued rejection of the claims based on Lin are inappropriate.

All outstanding matters having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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